Abstracts

A low-power 20 GHz static frequency divider with programmable input sensitivity

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A low-power frequency divider (divide-by-8) is described which operates up to frequencies in excess of 20 GHz with a supply voltage of 2.7 V. The circuit is implemented in a standard bipolar Silicon technology with a maximum f/sub T/ of 37 GHz. The total power dissipation is 57 mW, with 11 mW dissipated in the first divider stage. An innovative implementation of a Toggle flip-flop enables the input sensitivity to be adapted as a function of the input frequency, extending the operation range with respect to standard techniques. An AC simulation model for evaluation of the high frequency performance as a function of design parameters is introduced.

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